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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,260	03/15/2004	Ichiro Fujimori	13912US04	2251

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,260	FUJIMORI, ICHIRO	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Request for Continued Examination filed on 4/27/06 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 8-9, 12 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Puar et al (US. 6,356,497) in view of McCormack et al (US. 6,395,591).

Regarding claims 1 and 8-9, Puar (Fig. 5) discloses a system for reducing noise in a chip, the system comprising: a substrate layer (P substrate) integrated within the chip; a transistor well layer (N-Well) integrated within the chip; at least one transistor of a first transistor type (P-type) formed within the well layer; and a positive potential of a quiet voltage source Vdd (column 4, lines 59-63) that is coupled to the at least one transistor of the first transistor type.

Puar does not disclose that the transistor well layer (N-Well) is shielded by a shielding layer.

However, McCormack (Fig. 2) teaches the forming of a transistor within a transistor well layer and on a lightly doped (p-) substrate layer 50. The transistor well layer is isolated or shielded from the substrate 50 by a p type epitaxy layer 12 disposed

therebetween. The layer 12 functions as a shielding layer because it isolates the noise transfer to the substrate layer 50 from the noise generated during switching operations of the switches and power MOSFETs formed in the transistor well layer (column 4, lines 25-29). Accordingly, it would have been obvious to modify the device of Puar by forming the shielding layer between the substrate layer and the transistor well layer because such forming of the shielding layer would isolate the noise transfer to the substrate layer during switching operations of the switches and power MOSFETs.

Regarding claims 14-15, Puar (Fig. 5) further discloses a noisy voltage source 38 of positive (column 4, lines 59-63) coupled to a source of the transistor.

Regarding claim 12, McCormack (Fig. 2) further teaches that the shielding layer 12 is disposed between the substrate layer 10 and the transistor well layer 16/18/22.

4. Claims 1-10, 12, and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack et al (US. 6,395,591) in view of Puar et al (US. 6,356,497).

Regarding claims 1, 8-9 and 12, McCormack (Fig. 2) discloses a system for reducing noise in a chip (column 2, lines 45-50), the system comprising: a substrate layer 10 integrated within the chip; a transistor well layer 16/18/22 within the chip, which is isolated or shielded from the substrate layer 10 by a shielding layer 12; a transistor 30 of a first transistor type (P type) disposed within the transistor well layer 22, wherein the transistor well layer 22 is coupled to the shielding layer 12, and the shielding layer 12 is disposed between the substrate layer 10 and the transistor well layer 22.

McCormack does not disclose a positive potential of a quiet voltage source coupled to the transistor 30.

However, Puar (Fig. 5) teaches the forming of a system for reducing noise in a chip, the system comprising a transistor of P type disposed in a transistor well layer (N-Well) and having a positive potential Vdd of a quiet voltage source (column 4, lines 59-63) coupled to the transistor. Accordingly, it would have been obvious to couple a positive potential of a quiet voltage source to the transistor well layer (N-Well) of the transistor 30 of McCormack because such coupling of positive quiet voltage source to the transistor well layer would prevent the noise generated from the noisy substrate voltage, as taught by Puar (column 4, lines 55-65).

Regarding claims 2-7, McCormack (Fig. 2) further discloses a transistor 28 of a second transistor type (N type) disposed within the transistor well layer 16 and coupled to the shielding layer 12, wherein the transistor 28 has a transistor well layer 16 of P type is resistivity coupled to the shielding layer 12 of P type and has a first noisy voltage source 24 (column 3, lines 53-55) coupled to a source 17 of the transistor 28.

Regarding claim 10, McCormack (Fig. 2) further discloses that the transistor 30 has a transistor well layer 22 of N type is capacitively coupled to the shielding layer 12 of P type.

Regarding claims 14-15, Puar (Fig. 5) also teaches a noisy voltage 38 (column 4, lines 59-63) coupled to the transistor source of a first transistor type (P type).

5. Claims 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack et al and Puar et al as applied to claim 1 above, and further in view of Wei (US. 6,403,992).

McCormack discloses the shielding layer 12 is deep P-well, but not N-well which is capacitively coupled to the substrate layer 10.

However, Wei teaches the conventional of forming a transistor within a shielding layer of P-well, which is capacitively coupled to the N type substrate (Fig. 3), or a transistor within a shielding layer of N-well, which is capacitively coupled to the P type substrate (Fig. 4). Accordingly, it would have been obvious to form the shielding layer 12 of McCormack with either N type or P type because they both provide the benefits of eliminating substrate effect, as taught by Wei (column 1, lines 47-60).

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1-15 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-6 and 9-12 of U.S. Patent No. 6,995,431. Although the conflicting claims are not identical, they are not patentably distinct from each other because both base claim 1 of U.S. Patent and the instant application claim a system for reducing noise in a chip, the system comprising: a substrate layer; a transistor layer (a second well) integrated within the chip, which is shielded from the substrate layer by a shielding layer (first well); at least one transistor of a first transistor type that couples the transistor layer (a second well) to the shielding layer (first well); and a positive potential of a quiet voltage source that is coupled to the transistor of the first transistor type. Moreover, the claims in the instant application are either broader versions of the claims in U.S. Patent '431 or are obvious variations thereof. For example, claim 1 in U.S. Patent '431 claims "a second well...disposed within said first well; a first transistor disposed in said second well...", whereas claim 1 in the instant application claims "a transistor layer...is shielded...by a shielding layer;...a first transistor type that couples said transistor layer to said shielding layer", that shows no different meaning between these two elements. The facts are that the claims of the instant application and the U.S. Patent '431 have claimed the same goal and are not distinguished from each other.

Claims 2-15 of the instant application corresponds to claims 2-6 and 9-12 of the U.S. Patent '431.

Response to Arguments

8. Applicant argues that it would not be obvious to combine McCormack with Puar because McCormack fails to disclose "a shielding layer". According to Applicant, the P type epitaxy layer 12 does not function as "a shielding layer" for reducing noise in a chip.

This argument is not persuasive because of the following reasons:

First, the limitation of having "a shielding layer" functioning as reducing noise in a chip does not seem to be required by the claim language because it is not stated in the claims. It is the claims that define the claimed invention, and it is claims, not specifications that are anticipated or unpatentable. *Constant v. Advanced Micro-Devices Inc.*, 7 USPQ2d 1064. Therefore, the P type epitaxy layer would function as "a shielding layer" because this layer is disposed between the substrate layer 10 and the transistor well layers for isolating or shielding the transistor well layers from the substrate layer 10. And

Second, in contrary to Applicant's assertions, McCormack clearly states at column 4, lines 25-29 that "Digital switches and power MOSFET **generated substrate noise** during switching operations. In particular, power MOSFETs, typically used to provide one to three amperes of output current, can generate a substantial amount of shoot-through current." Therefore, the P type epitaxy layer 12 would inherently function as "a shielding layer" for reducing the noise transfer to the substrate layer 10 from the noise generated during switching operation of the switches and power MOSFETs formed in the transistor well layers because the epitaxy layer 12 is disposed between

the substrate layer 10 and the transistor well layers to isolate the substrate layer 10 from the transistor well layers.

Applicant is noted that since the examiner presents evidence or reasoning tending to show inherency, the burden shifts to Applicant to show an unobvious different. Therefore, if Applicant belies that the P type epitaxy layer 12 would not function as an isolating layer or "shielding layer" even though it is disposed between the substrate layer 10 and the transistor well layers, then Applicant is requested to support that position with facts.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PC
June 12, 2006

PHAT X. CAO
PRIMARY EXAMINER